Ahmed Z. Ghonem

ASIC and SoC Design Engineer

Over five years of experience in ASIC design, from architecture and RTL to GDSII. Successfully taped-out four SoCs in deep submicron technology, achieving optimal PPA results. Skilled in leveraging industry-standard EDA tools, complemented by proficiency in scripting with Python and TCL. Strong collaborator with excellent communication skills, committed to building consensus across multidisciplinary teams and pushing the boundaries of SoC design.

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TECHNICAL SKILLS

Analytical	Deep understanding of low-power design across the stack from architecture, RTL, synthesis, PPA, to IP and hierarchical PnR .
ASIC - Flow Tools	Cadence (Xceluim, Genus, Innovus, Tempus, voltus), Synopsys (VCS and DC, ICC II), Vivado and QuestaSim.
IC Design Tools	Cadence virtuoso, Mentor IC-Station, layout editor, x-Layout, DRC, LVS, PEX, and post-layout simulation and verification.
Languages	Verilog, SystemVeilog, Python (NNs, PyTorch), Matlab, C++, Verilog-A, Latex, TCL, PERL and bash scripting.

PROFESSIONAL EXPERIENCE

Graduate Research Associate
Electroscience Lab - The Ohio State University

10/2021 - Present — *Columbus, Ohio, USA*

Achievements/Tasks

- Developing Neuromorphic Processor for efficient computing including algorithmic modeling in Python and hardware design in SystemVerilog.
- Designed and verified an SPI-based programming interface for an eFPGA and integrated it within a large SoC through an SPI-TileLink bridge.
- Built the entire Digital Physical Design flow infrastructure for GF22nm (i.e., Synthesis, APR scripts, physical verification (DRC, LVS and DFM)).
- Derived the physical design of an SoC in a bottom-up approach; SoC included RISC-V processors, TileLink Bus, eFPGA, and security accelerators.
- Created a custom package and an evaluation board for the fabricated SoC. Thanks to the custom board, the chip achieved a speed of 650MHz.
- Established the testing setup of the evaluation board leveraging testing FPGAs, a logic analyzer, and an oscilloscope.

Contact : Dr. Eslam Tawfik - tawfik.10@osu.edu

Research Engineer III
Agency for Science, Technology and Research (A*STAR)

10/2020 - 10/2021 — *Singapore*

Achievements/Tasks

- Integrated and verified a Deep Learning Accelerator (NVDLA) through an AXI4 interface into a RISCV-based SoC.
- Led the design and verification of an SoC based on TSMC22ULL technology. The SoC, ECSDoT, surpassed state-of-the-art energy efficiency for AI workloads, featuring a RISC-V processor, high-performance DL/AI accelerator, on/off-chip communication (JTAG, UART, uDMA), and more.
- Established an FPGA - RaspberryPi - wearable demo emulating the created SoC, where activity recognition was applied as a use case.

Contact : Dr. Lin Jie - lin-j@i2r.a-star.edu.sg

Researcher
Nanyang Technological University (NTU)

03/2019 - 09/2020 — *Singapore*

Achievements/Tasks

- Spearheaded the design, verification, and physical implementation of an SoC using UMC40ULP technology. The SoC, ECS- α, comprises a 32-bit RISC-V core, a specially designed ReRAM controller, **4Mb ReRAM,** and an energy-efficient convolution engine (ML Accelerator).
- Led the design, verification, and testing of an SoC on TSMC22ULL technology. The SoC, ECS- 1, featured a RISC-V processor, an MRAM controller, **16Mb MRAM,** and in-house developed energy-efficient 8-bit neural processing engine (ML Accelerator).
- Designed custom SRAM readout circuit using thin-film transistors for flexible electronics.

Contact : Dr. Mohamed Sabry - msabry@ntu.edu.sg

PROFESSIONAL EXPERIENCE

Research Assistant - R&D Engineer
American University in Cairo - Helic, SA

10/2018 - 03/2019 *Cairo, Egypt*

Achievements/Tasks

- Developed the first version of Model Order Reduction (MOR) tool using MATLAB delivered to Mentor Graphics, Siemens.
- Provided algorithmic advancement for MOR and EDA software tools for faster and more accurate IP and SOC development and modeling.
- Delivered a knowledge exchange session at Helic,SA Greece.

Contact : Dr. Yehea Ismail - y.ismail@aucegypt.edu

Research Assistant
ONE Lab - Cairo University

07/2017 - 09/2018 *Cairo, Egypt*

Achievements/Tasks

- Developed the first compact model using Verliog-A for Triboelectronic Nanogenerators (TENGs) energy harvesters.
- Proposed and formulated 2-new modes of TENGs and proved the results using analytical FEM modelling vs mathematical and compact modelling.
- Demonstrated the results in the format of 1 Journal Paper, and 3 IEEE Conference Papers.

Contact : Dr. Hassan Mostafa - hmostafa@uwaterloo.ca

EDUCATION

M.Sc. in Electrical & Computer Engineering
The Ohio State University

09/2021 - 12/2023 *GPA: 3.9, Graduate Assistantship Scholarship*

B.Sc. in Nanoelectronics Engineering
University of Science and Technology - Zewailcity

2013 - 2018 *GPA: 3.6, University Fellowship Recipient*

SELECTED PUBLICATIONS

IEEE SOCC 2023 Conference
A 3.6TOPS/W Deep Learning Accelerated SoC with 16 Mbit On-Chip Dynamically Gated MRAM for Ultra-Low Power AIoT
2023

IEEE International Computer Engineering Conference
Ultra Low-Power Encryption/Decryption Core for Lightwieght IoT Applications
2019

IEEE MWSCAS 2017 Conference
Characterization and model validation of triboelectric nanogenerators using Verilog-A
2017

IEEE MWSCAS 2018 Conference
In-Out Cylindrical Triboelectric Nanogenerators Based Energy Harvester
2018

Design, Automation and Test in Europe (DATE) Conference
Fledge: Flexible edge platforms enabled byin-memory computing
2020

Design, Automation and Test in Europe (DATE) Conference
Quantifying the benefits of Monolithic 3D Computing Systems Enabled by TFT and RRAM
2020

ACHIEVEMENTS

Microelectronics Olympiad - USA (06/2023)
First place over the USA chapter of Synopsys microelectronics Olympiad.

IEEE HOST Microelectronics Challenge (06/2022)
Placing first in the SoC security challenge.

Founder of Nanotechnology Club - ZC (2016 - 2018)
Educating new students on the major and the market trends in the industry.

Zewailcity Research Excellence Award (2018)
A prestigious award given for outstanding research efforts during undergraduate studies.

MEMS Design Contest - Semi finalist (02/2017 - 01/2018)
Chosen as semi-finalist in" MEMS Design Contest" held by Cadence. XFAB and Coventor.

Best poster award (2015 - 2016)
First place out of 50 posters exhibiting research and scientific work at ZC 1st (2015) and 2nd (2016) undergraduate research conference.